



Advances in Analog and RF IC Design for Wireless Communication Systems: Chapter 10. Interleaving of Successive-Approximation Register ADCs in Deep Sub-Micron CMOS Technology

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This paper reviews recent developments of interleaved Successive Approximation Analog-to-Digital converters (SAR) in deep sub-micron CMOS technologies. The discussion covers design tradeoffs and degrees of freedom related to the impact of extensive interleaving with many SAR units on bandwidth, noise, linearity, and spurious performance. The impact of interleaving mismatches on representative broadband and multi-carrier narrowband signals is also discussed. Next, two examples are given demonstrating how interleaving with many ADCs can be transformed from a weakness to a strength. The first example concerns low spurious performance enabled by redundant SAR converters and randomization of their operation. The second example presents spectral sensing techniques.

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