



The gm/ID Methodology, a sizing tool for low-voltage analog CMOS Circuits: The semi-empirical and compact model approaches (Analog Circuits and Signal Processing)

Paul Jespers

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IC designers appraise currently MOS transistor geometries and currents to compromise objectives like gain-bandwidth, slew-rate, dynamic range, noise, non-linear distortion, etc. Making optimal choices is a difficult task. How to minimize for instance the power consumption of an operational amplifier without too much penalty regarding area while keeping the gain-bandwidth unaffected in the same time? Moderate inversion yields high gains, but the concomitant area increase adds parasitics that restrict bandwidth. Which methodology to use in order to come across the best compromise(s)? Is synthesis a mixture of design experience combined with cut and tries or is it a constrained multivariate optimization problem, or a mixture? Optimization algorithms are attractive from a system perspective of course, but what about low-voltage low-power circuits, requiring a more physical approach? The connections amid transistor physics and circuits are intricate and their interactions not always easy to describe in terms of existing software packages.

The gm/ID synthesis methodology is adapted to CMOS analog circuits for the transconductance over drain current ratio combines most of the ingredients needed in order to determine transistors sizes and DC currents.

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Martina Joseph:

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